FIG. 1

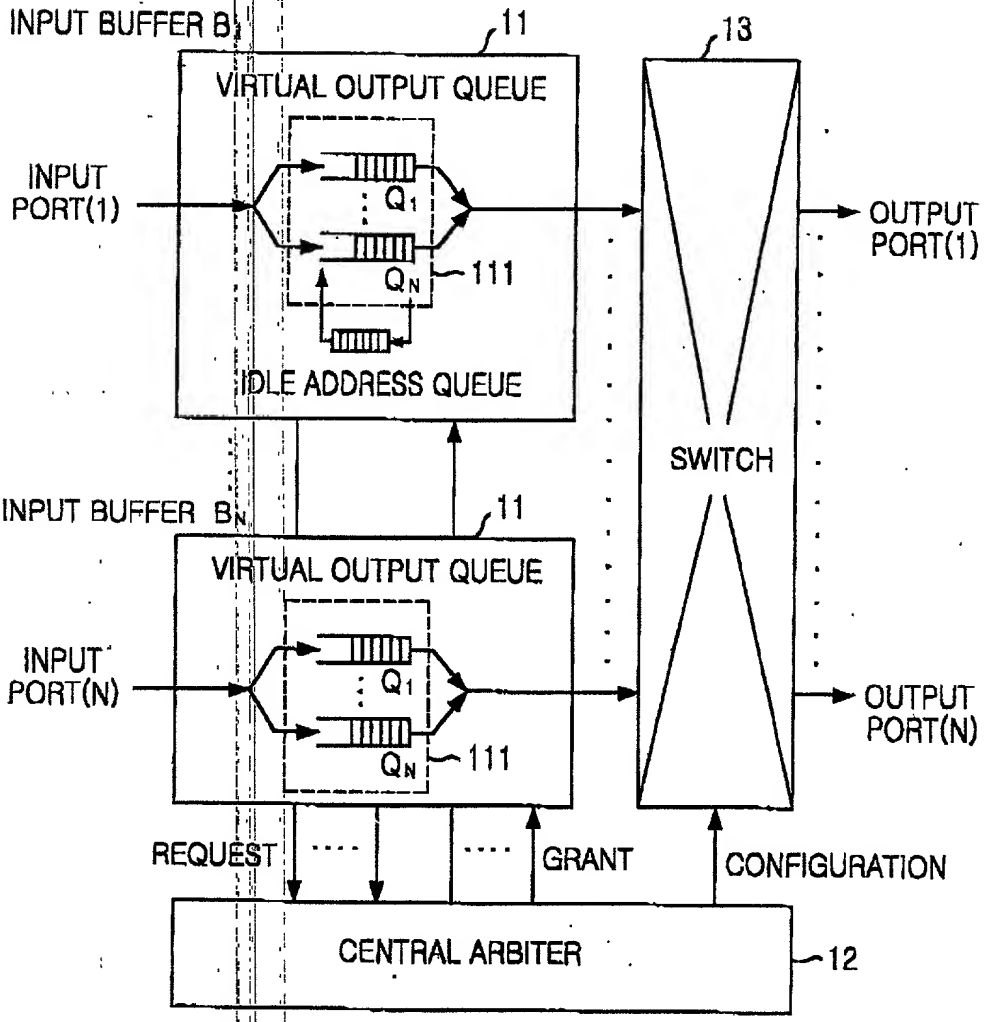

INPUT BUFFER B1
11
13
VIRTUAL OUTPUT QUEUE
INPUT PORT(1)
Q1
QN
111
IDLE ADDRESS QUEUE
OUTPUT PORT(1)
SWITCH
INPUT BUFFER BN
11
VIRTUAL OUTPUT QUEUE
INPUT PORT(N)
Q1
QN
111
OUTPUT PORT(N)
REQUEST
GRANT
CONFIGURATION
CENTRAL ARBITER
12

FIG. 2

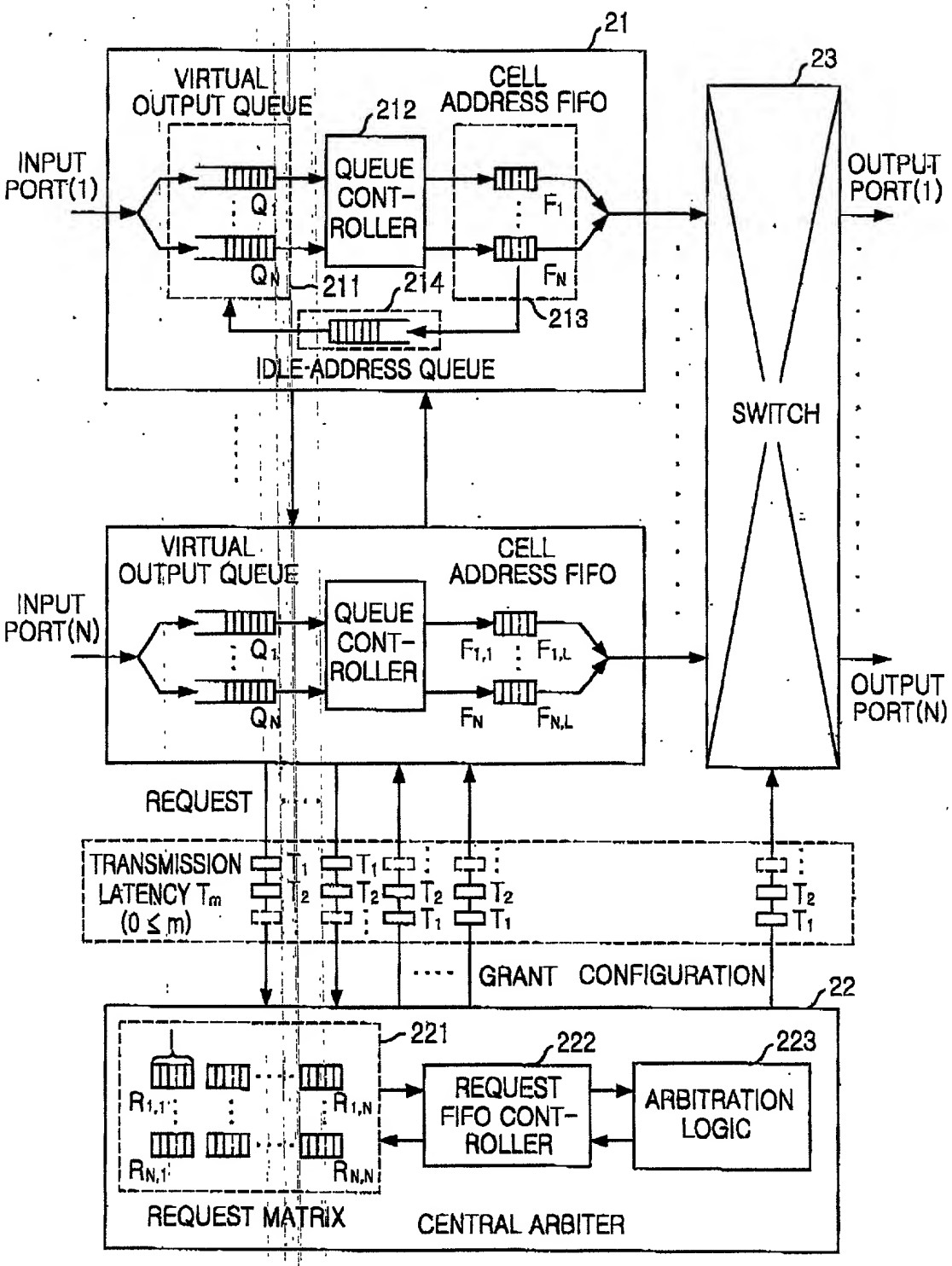

21
VIRTUAL OUTPUT QUEUE
CELL ADDRESS FIFO
212
INPUT PORT(1)
QUEUE CONT-ROLLER
Q1
QN
F1
FN
211
214
213
IDLE-ADDRESS QUEUE
23
OUTPUT PORT(1)
SWITCH
VIRTUAL OUTPUT QUEUE
CELL ADDRESS FIFO
INPUT PORT(N)
QUEUE CONT-ROLLER
Q1
QN
F1,1
F1,L
FN
FN,L
OUTPUT PORT(N)
REQUEST
TRANSMISSION LATENCY Tm (0 ≤ m)
T1
T2
GRANT
CONFIGURATION
22
221
222
223
R1,1
R1,N
RN,1
RN,N
REQUEST FIFO CONT-ROLLER
ARBITRATION LOGIC
REQUEST MATRIX
CENTRAL ARBITER

FIG. 3

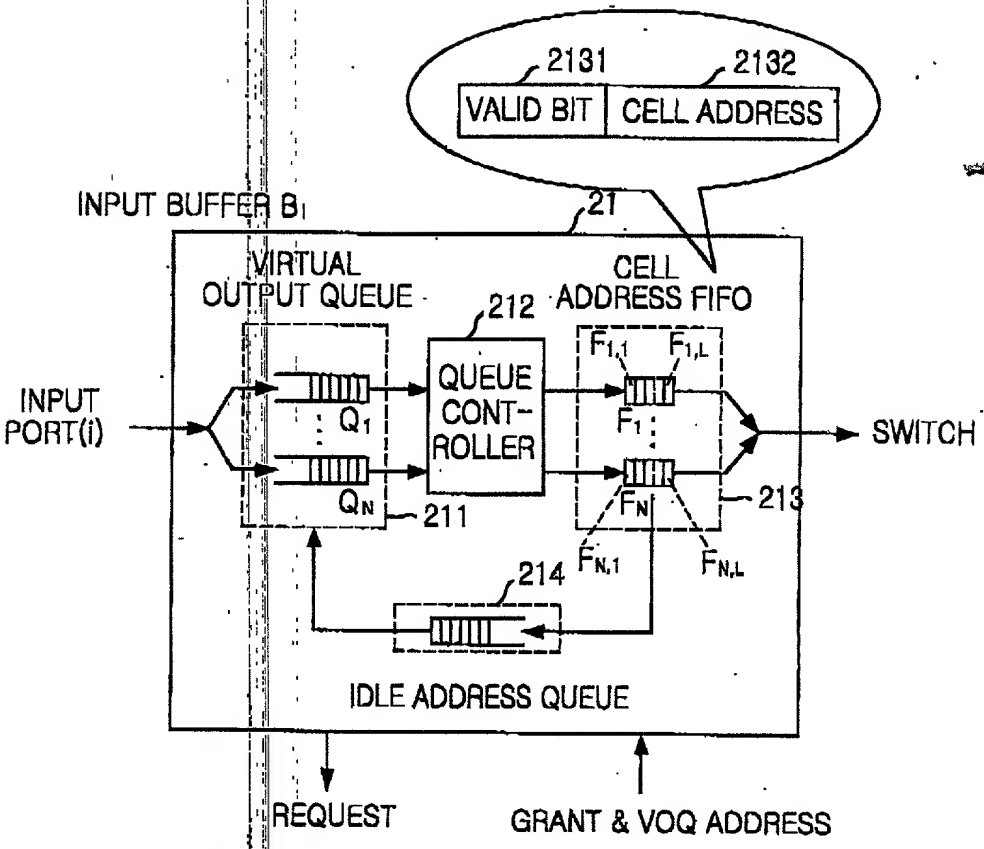

2131
2132
VALID BIT
CELL ADDRESS
INPUT BUFFER Bi
21
VIRTUAL OUTPUT QUEUE
CELL ADDRESS FIFO
212
INPUT PORT(i)
Q1
QN
211
QUEUE CONT-ROLLER
F1,1
F1,L
F1
FN
213
FN,1
FN,L
SWITCH
214
IDLE ADDRESS QUEUE
REQUEST
GRANT & VOQ ADDRESS

FIG. 4

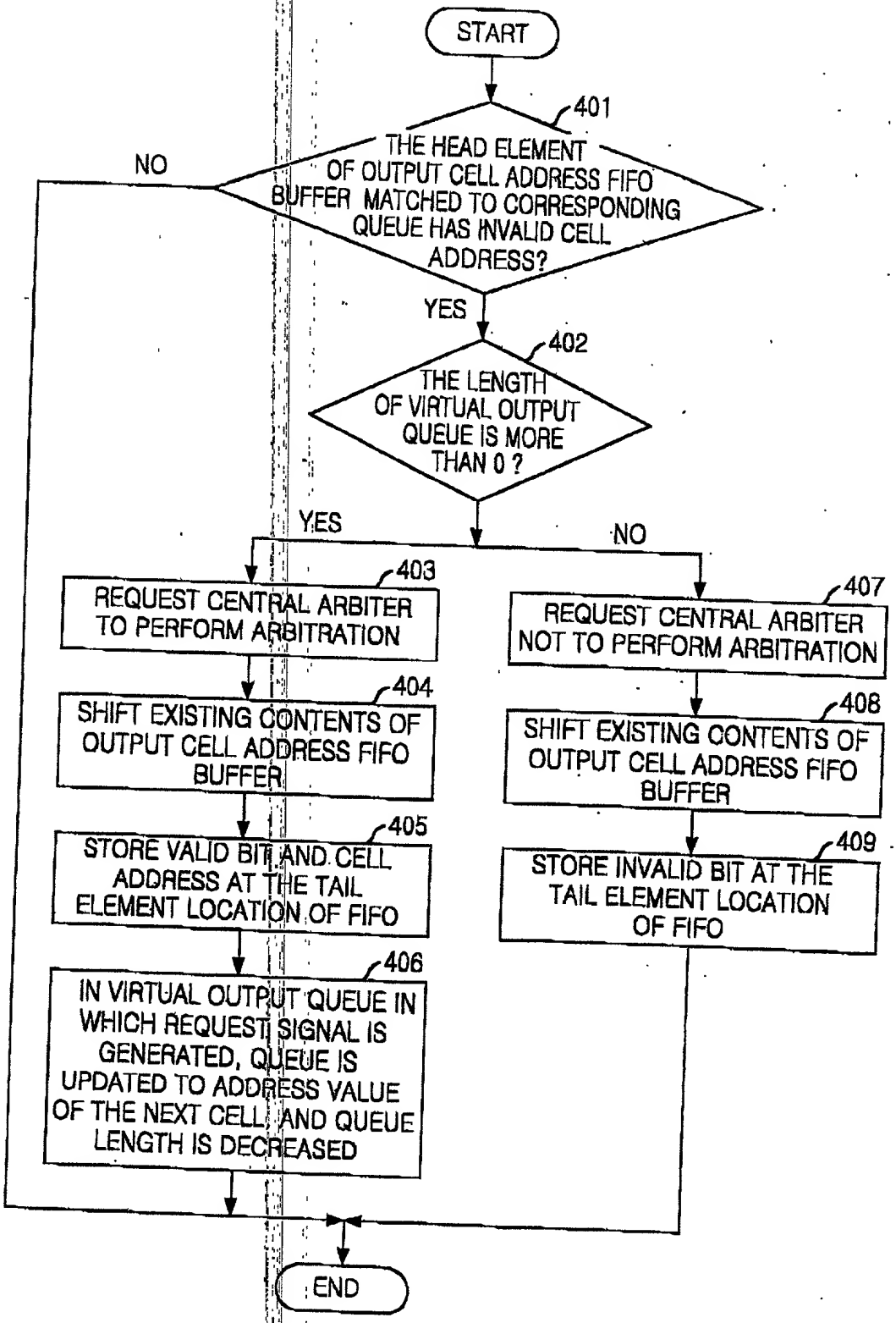

START
401
THE HEAD ELEMENT OF OUTPUT CELL ADDRESS FIFO BUFFER MATCHED TO CORRESPONDING QUEUE HAS INVALID CELL ADDRESS?
NO
YES
402
THE LENGTH OF VIRTUAL OUTPUT QUEUE IS MORE THAN 0 ?
YES
NO
403
REQUEST CENTRAL ARBITER TO PERFORM ARBITRATION
404
SHIFT EXISTING CONTENTS OF OUTPUT CELL ADDRESS FIFO BUFFER
405
STORE VALID BIT AND CELL ADDRESS AT THE TAIL ELEMENT LOCATION OF FIFO
406
IN VIRTUAL OUTPUT QUEUE IN WHICH REQUEST SIGNAL IS GENERATED, QUEUE IS UPDATED TO ADDRESS VALUE OF THE NEXT CELL, AND QUEUE LENGTH IS DECREASED
407
REQUEST CENTRAL ARBITER NOT TO PERFORM ARBITRATION
408
SHIFT EXISTING CONTENTS OF OUTPUT CELL ADDRESS FIFO BUFFER
409
STORE INVALID BIT AT THE TAIL ELEMENT LOCATION OF FIFO
END

FIG. 5

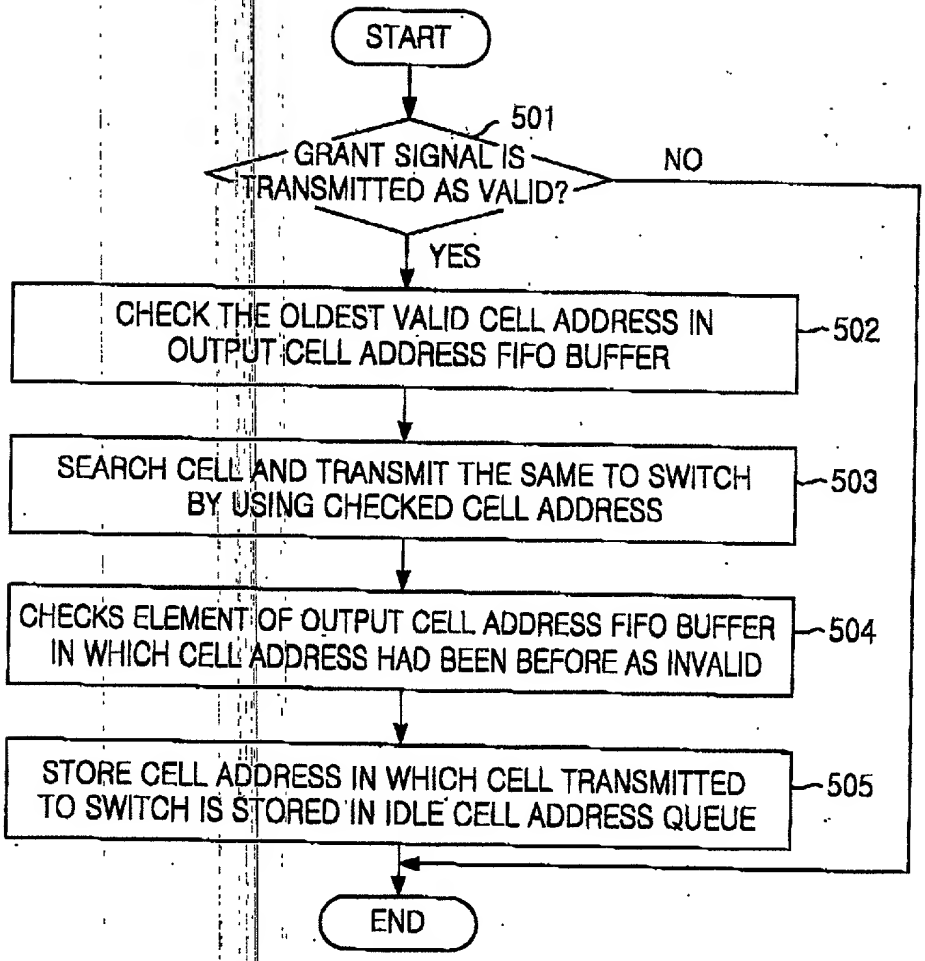

START
501
GRANT SIGNAL IS TRANSMITTED AS VALID?
NO
YES
CHECK THE OLDEST VALID CELL ADDRESS IN OUTPUT CELL ADDRESS FIFO BUFFER
502
SEARCH CELL AND TRANSMIT THE SAME TO SWITCH BY USING CHECKED CELL ADDRESS
503
CHECKS ELEMENT OF OUTPUT CELL ADDRESS FIFO BUFFER IN WHICH CELL ADDRESS HAD BEEN BEFORE AS INVALID
504
STORE CELL ADDRESS IN WHICH CELL TRANSMITTED TO SWITCH IS STORED IN IDLE CELL ADDRESS QUEUE
505
END

FIG. 6

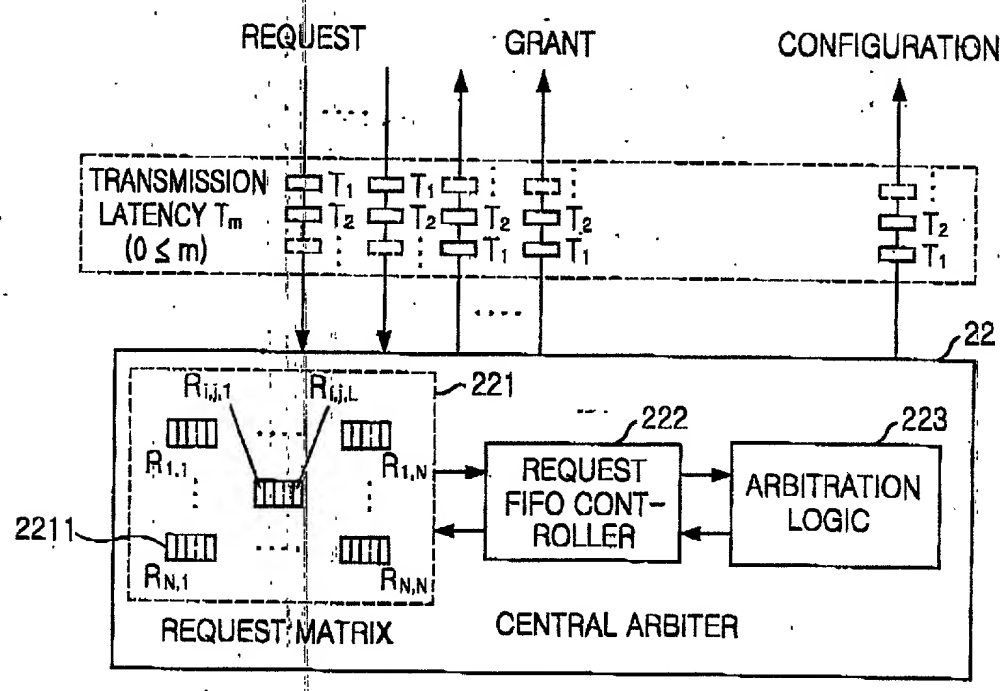

REQUEST
GRANT
CONFIGURATION
TRANSMISSION LATENCY T_m ($0 \le m$)
T_1
T_2
22
221
222
223
$R_{i,j,1}$
$R_{i,j,L}$
$R_{1,1}$
$R_{1,N}$
$R_{N,1}$
$R_{N,N}$
2211
REQUEST FIFO CONTROLLER
ARBITRATION LOGIC
REQUEST MATRIX
CENTRAL ARBITER

FIG. 7

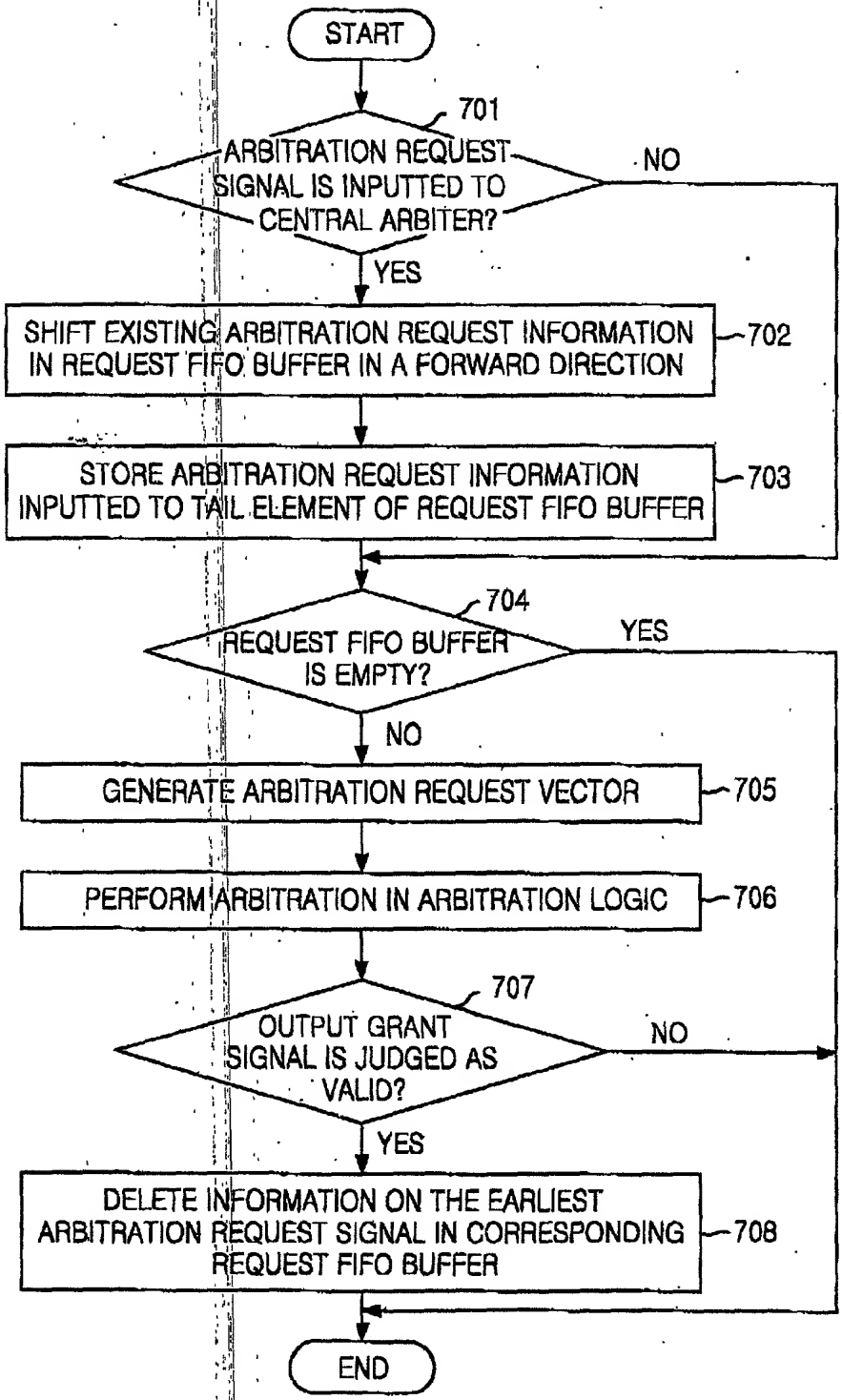
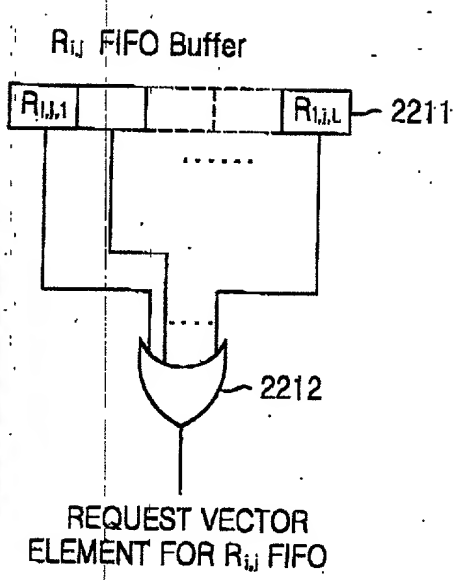

START
701
ARBITRATION REQUEST SIGNAL IS INPUTTED TO CENTRAL ARBITER?
NO
YES
SHIFT EXISTING ARBITRATION REQUEST INFORMATION IN REQUEST FIFO BUFFER IN A FORWARD DIRECTION
702
STORE ARBITRATION REQUEST INFORMATION INPUTTED TO TAIL ELEMENT OF REQUEST FIFO BUFFER
703
704
REQUEST FIFO BUFFER IS EMPTY?
YES
NO
GENERATE ARBITRATION REQUEST VECTOR
705
PERFORM ARBITRATION IN ARBITRATION LOGIC
706
707
OUTPUT GRANT SIGNAL IS JUDGED AS VALID?
NO
YES
DELETE INFORMATION ON THE EARLIEST ARBITRATION REQUEST SIGNAL IN CORRESPONDING REQUEST FIFO BUFFER
708
END

FIG. 8


$R_{i,j}$ FIFO Buffer
$R_{i,j,1}$
$R_{i,j,L}$
2211
2212
REQUEST VECTOR
ELEMENT FOR $R_{i,j}$ FIFO